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DESIGN STUDY

Compute nodes under memory allocation: 180 servers split across two manufacturers for a genomics refresh

Complete design on current platforms

CAPABILITY	INDUSTRY	SETTING
Strategic Resourcing	Life Sciences	Genomics research institute
DOCUMENT	**VERSION**	**DATE**
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WRITTEN BY

Avinash Dhinakaran, Principal Integration Architect

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Document control

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Sign-off	"An engagement under this design is signed by the practice lead before any build proceeds."		

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CONVENTIONS

Source tags. [S] figure or clause read from the vendor's, analyst's or standards body's own current page on Sep 24, 2026, or on Sep 27, 2026 where the text says so · [S*] figure from the page summary where the page itself could not be opened · [A] assumption about the typical buyer, to be confirmed by the signing engineer · [T] design target taken from the design's stated outcome or derived from it. Every figure carries at least one tag. No figure comes from any prior engagement, file or asset. A row with more than one tag is counted once: as a published figure if any tag is [S] or [S*], otherwise as an assumption if any tag is [A], otherwise as a design target.

Table 1. Revision history

Date	Version	Change
Sep 27, 2026	`1.0`	First issue.
Oct 10, 2026	`1.1`	Approval line now reads: approved by the Founder, issued by Symbeeo. Avinash Dhinakaran remains the author.

1 · Scope

Who it is for. The head of research computing at a genomics institute who has a signed server comparison, a funded refresh and a grant deadline, and now has to get 180 memory-heavy nodes delivered in a year when server memory is on allocation and re-priced every quarter.

Typical buyer [A]. A genomics research institute running a sequencing-analysis cluster. The refresh replaces 180 compute nodes: 2U, two sockets, 1.5 TB of DDR5 per node (24 × 64 GB), local NVMe scratch. Need-by date on the loading dock: week 40 from comparison sign-off [A]. The published comparison found two conforming platforms and ranked them within its tolerance of each other [A].

What is in. BOM baseline and criticality classes for both platforms; the split between the two manufacturers; one authorized channel per manufacturer; lead-time and price control from quote to delivery; provenance at receipt. **What is out.** The comparison itself; the cluster design and scheduler; rack, power and cooling (DC design studies); installation, which runs under SRA-RES-001 §4.8 once the nodes are received.

Assumptions. Both platforms pass the institute's own benchmark within 5 % of each other [A], so the comparison treats them as interchangeable. Each manufacturer is bought through one distributor that manufacturer authorizes [A]. The institute has no long-term memory agreement of its own [A].

Related documents, read Sep 24, 2026. SRA-RES-001 · SDD-RES-001 · STP-RES-001 · Dell PowerEdge R7725 product page (`https://www.dell.com/en-us/shop/dell-poweredge-servers/new-poweredge-r7725-rack-server/spd/poweredge-r7725/pe_r7725_tm_vi_vp_sb`) · Cisco UCS C245 M8 Rack Server data sheet, updated Mar 16, 2026 (`https://www.cisco.com/c/en/us/products/collateral/servers-unified-computing/ucs-c-series-rack-servers/ucs-c245-m8-rack-server-ds.html`) · TrendForce, Apr 15, 2026 (`https://www.trendforce.com/presscenter/news/20260415-13013.html`) · TrendForce, Jul 9, 2026 (`https://www.trendforce.com/presscenter/news/20260709-13140.html`) · Dell Systems Management Overview Guide 26.0, Secured Component Verification (`https://www.dell.com/support/manuals/en-us/dell-dss-9600/smog_26.0/secured-component-verification?guid=guid-7bda2c6a-9248-4ce3-a8ed-bedccd7637e1&lang=en-us`) · NIST SP 1800-34 (`https://csrc.nist.gov/pubs/sp/1800/34/final`) · ECMA-424 (`https://ecma-international.org/publications-and-standards/standards/ecma-424/`).

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1c · Public implementations this design follows

Table 2. Public implementations this design follows

Implementation	Who published it · date	What it settles for this design	URL
NIST SP 1800-34, Validating the Integrity of Computing Devices	NIST NCCoE · final, December 2022 · published standard, used to build our own design	A published, built demonstration that an acquirer can verify the internal components of servers it receives are genuine and untampered, using information the vendor stores in the device; §4.5's receipt check is that pattern	https://csrc.nist.gov/pubs/sp/1800/34/final
Secured Component Verification on PowerEdge	Dell · Systems Management Overview Guide 26.0, March 2026, Rev. A05 (read Sep 27, 2026) · vendor documentation, used to build our own design	Dell signs a Platform Certificate and a Firmware Certificate at factory assembly and stores them in the server; the SCV application checks the received server against them; R10 uses it for the Dell half	https://www.dell.com/support/manuals/en-us/dell-dss-9600/smog_26.0/secured-component-verification?guid=guid-7bda2c6a-9248-4ce3-a8ed-bedccd7637e1&lang=en-us
TrendForce server-component and DRAM releases	TrendForce · Apr 15, 2026 and Jul 9, 2026 · vendor documentation (market analyst releases), used to build our own design	The market record the float rule (R6) and price gate (R7) are sized against: CPU and PCB lead times near one year (R8); server DRAM contract prices up 13–18 % quarter on quarter in 3Q26, falling on buyers without long-term agreements (R9)	https://www.trendforce.com/presscenter/news/20260709-13140.html
A US university research-computing cluster, node buy-in	The university · notice dated Mar 30, 2026 (read Sep 27, 2026) · public deployment	A research-computing cluster that sells compute nodes to its researchers stopped publishing node prices from Mar 30, 2026 because pricing "is fluctuating regularly due to industry-wide supply constraints", and quotes each node order before it is placed. It offers Intel and AMD node options side by side. It is the buyer-side condition this design's price gate (R7), quote validity (R13) and two-platform split (R2) are built for	https://campuscluster.illinois.edu/access/buy-compute/

The Cisco platform's lower published memory speed is carried into R3. The university cluster row is the only public deployment found; no genomics institute's published refresh split across two manufacturers was found as of Sep 27, 2026.

2 · Requirements register

Table 3. Requirements register

#	Requirement	Value	Source
R1	Nodes delivered	180, by week 40	[T]
R2	Split between manufacturers	90 and 90; each manufacturer able to absorb the whole order if the other fails	[A]
R3	Node floor both platforms must meet	2U, 2 sockets, ≥ 64 cores per socket, 24 DIMM slots, DDR5 at ≥ 6000 MT/s	[A]

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#	Requirement	Value	Source
R4	Platform 1	Dell PowerEdge R7725: 2U, 2 × AMD EPYC 9005 up to 192 cores per socket, DDR5-6400, iDRAC10; PSU options 800 W to 3200 W	[S] Dell
R5	Platform 2	Cisco UCS C245 M8: 2RU, 2 × 5th or 4th Gen AMD EPYC up to 160 cores per socket, 24 DDR5 DIMM slots at up to 6000 MT/s with 5th Gen, up to 6 TB; Intersight, IMC, UCS Manager	[S] Cisco
R6	Float on every class-A line at order	need-by minus (order date + quoted lead time) ≥ 4 weeks	[A]; SRA-RES-001 R6
R7	Price gate	a line re-priced > 5 % above the comparison is held for the buyer's approval	[A]; SRA-RES-001 R8
R8	Component lead times on record	CPUs and PCBs near one year; PMICs 35–40 weeks; BMC chips 21–26 weeks	[S] TrendForce, Apr 15, 2026
R9	Server DRAM contract price, 3Q26	+13–18 % quarter on quarter; increases fall on buyers without long-term agreements	[S] TrendForce, Jul 9, 2026
R10	Provenance at receipt	100 % of nodes: serial matched to ship notice, seal, entitlement, firmware read; Dell nodes also SCV-verified	[T]; [S] Dell SCV
R11	Promised-date change in the register	≤ 1 business day after acknowledgment	[A]; SRA-RES-001 R7
R12	Bill of materials attached where the manufacturer publishes one	CycloneDX 1.7, ECMA-424 2nd edition (December 2025)	[S] Ecma
R13	Quote validity requested on memory lines	≥ 14 days	[A]
R14	Manufacturer end-of-support after delivery	≥ 5 years	[A]; SRA-RES-001 R9

Fourteen rows; six carry a vendor, analyst or standards-body figure (one beside a design target), seven are design assumptions or SRA-RES-001 values, one is a design target.

3 · Architecture overview

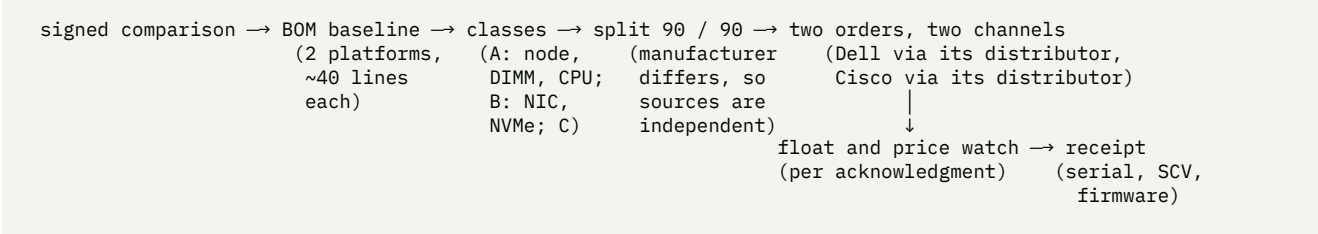


Figure 1. Two-manufacturer sourcing flow

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One register holds both platforms' lines. The split is the continuity plan: each manufacturer is the other's alternate, so an allocation cut moves quantity between two open orders instead of starting a new qualification.

Table 4. Architecture overview

Line family	Class	Why	Source depth
Node chassis with CPUs	A	CPU and PCB lead times near one year (R8)	2: one per manufacturer
DDR5 RDIMMs, 64 GB	A	price moves 13–18 % a quarter (R9); 4,320 DIMMs in the order	2: one per manufacturer, factory-fitted
NVMe scratch drives	B	alternates on both manufacturers' lists	1, alternate pre-qualified
Network adapters	B	must match the fabric in the cluster design	1, alternate pre-qualified
Rails, cables, power cords	C	interchangeable	bought on price
Support contracts	B	entitlement must be live at receipt (R10)	1 per manufacturer

4 · Design by subsystem

4.1 BOM baseline.

Two bills of materials, one per platform, about 40 lines each [A], frozen at comparison sign-off. Each platform's configuration meets R3: the R7725 at DDR5-6400 [S] and the C245 M8 at up to 6000 MT/s with 5th Gen EPYC [S] both clear a 6000 MT/s floor; core counts of up to 192 [S] and up to 160 [S] per socket both clear 64. Rejected: setting the floor at DDR5-6400 — it would disqualify the second platform and leave a single source on every class-A line.

4.2 Allocation.

90 nodes to each manufacturer [A], each through one authorized distributor. The two sources are independent because the manufacturer differs (SRA-RES-001 §4.3). Memory is ordered factory-fitted, never as loose DIMMs, so the DIMM line inherits the node's channel and provenance [A]. Rejected: 180 nodes from one manufacturer at a volume discount — one allocation notice would stop the whole cluster.

4.3 Lead time.

Quoted lead time, quote expiry and promised date recorded per line at order (R6, R13). With need-by at week 40 [T], a quoted lead time above 36 weeks breaks the 4-week float [T] derived; that line is escalated before the order is placed, and quantity moves to the other manufacturer if its quote holds float. Every acknowledgment recomputes float; under 2 weeks escalates, under zero moves quantity (SRA-RES-001 §4.5).

4.4 Price.

TrendForce puts 3Q26 server DRAM contract prices up 13–18 % quarter on quarter, the increases falling on buyers without long-term agreements [S]. The institute has none [A]. The low end of that range is above the 5 % gate [T] derived, so any memory-bearing quote that crosses a quarter boundary before the order is placed should be expected to trip R7. The design therefore places both orders inside the validity of the first firm quotes, and records the buyer's approval where it does not.

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4.5 Receipt and provenance.

Per node: serial scanned against the ship notice; seal inspected; support entitlement confirmed on the manufacturer's portal; BIOS and management-controller firmware read and recorded [A]. Dell nodes: Secured Component Verification run against the Platform and Firmware Certificates stored in the server at factory assembly [S]. Cisco nodes: the same checks without a signed platform certificate, which this document does not claim for that platform [A]. Where either manufacturer publishes a bill of materials for the shipped configuration, it is attached in CycloneDX 1.7 form [S] ECMA-424.

4.6 Register fields.

Per SRA-RES-001 §4.3 and SDD-RES-001 §6.1: line, class, manufacturer, channel and its authorization evidence, quote date, quoted lead time, quote expiry, price against the comparison, promised date, float, serial, provenance result.

5 · Failure behavior

Table 5. Failure behavior

Failure	Behavior	Source
One manufacturer cuts allocation	the other manufacturer's order is increased toward 180; float recomputed; buyer told the same day	[A]
Quoted lead time on a node line > 36 weeks	float < 4 weeks; quantity moves to the other manufacturer before order	[T] derived from R1, R6
Memory re-priced above 5 %	order held; buyer approves or quantity shifts to the lower-priced platform	[A]
Node fails SCV at receipt	quarantined, never racked; return raised; replacement ordered on the same line	[A]
Entitlement not live at receipt	node held at staging until the manufacturer corrects the contract	[A]
Both manufacturers slip past week 40	the cluster starts on the nodes received; the grant timeline is re-planned with the buyer	[A]

6 · Limits

- The two platforms are interchangeable only because R3 is written to a 6000 MT/s floor; a workload that measurably needs DDR5-6400 collapses the design to one source per line.
- TrendForce figures are component lead times and contract-price trends, not either manufacturer's quote for this order; the quoted lead time on the day decides R6.
- SCV covers the Dell half only; the Cisco half is checked by serial, seal, entitlement and firmware, not by a signed platform certificate.
- 4,320 DIMMs is 180 × 24; the figure assumes every slot populated, which the cluster design may change.
- No figure here has been measured.

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7 · Lessons learned

None yet — this is a design study; populated after the first build against it.

8 · The author

WRITTEN BY

Avinash Dhinakaran

Principal Integration Architect

iSAQB Certified Professional for Software Architecture – Advanced Level (CPSA-A), Oracle Certified Consultant – Value Chain Planning, Master Data Management, SCM Cloud

Signed off by Edwin Ozer, Founder.

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SYMBEEO

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Figures are as published by their sources on the dates given in this document; figures marked [A] are assumptions.

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